AMENDMENTS TO THE CLAIMS

The following listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1-20. (Cancelled)

21. (Currently Amended) Method according to claim [[19]]41 further comprising:

breaking the required linear frequency versus voltage curve into several sections over either constant or non-constant voltage intervals;

selecting for each section a corresponding element tuned by the tuning voltage giving the same frequency variation over said section; and

submitting each element tuned by the tuning voltage to a specific voltage, deduced from a loop filter output voltage, to activate each element in the same voltage interval as the corresponding section of each element.

22. (Cancelled).

23. (Currently Amended) Method according to claim [[19]]41, wherein the switching operation of the voltage-controlled oscillator from the linear-high-gain mode to the zero-gain mode comprises:

isolating the elements tuned by the tuning voltage from respective controlling voltages when the phase locked loop is locked;

comparing each element tuned by the tuning voltage to a reference voltage to determine if the value of each element is at a maximum or a minimum when the phase locked loop is locked;

depending on the result of this comparison, switching each element value to the maximum or to the minimum; and

freezing the elements tuned by the tuning voltage in the state previously obtained to activate the zero-gain mode for the voltage-controlled oscillator.

24. (Currently Amended) ~~Method according to claim 20,~~Method for analogue self calibrating of a phase locked loop circuit including a phase frequency detector, a charge pump, a loop filter, a voltage-controlled oscillator, including elements tuned by a tuning voltage, the method comprising:

comparing a frequency of an output signal of the voltage-controlled oscillator of the phase locked loop circuit with a reference signal frequency entering in the phase frequency detector;

switching a voltage-controlled oscillator operating mode to a linear-high-gain mode to enable a first frequency tuning operation that includes targeting a linear frequency versus voltage curve to vary the frequency of the output signal within a frequency locking range; and

after locking to a frequency with said first frequency tuning operation, switching said voltage-controlled oscillator operating mode to a zero-gain mode while keeping the frequency of the output signal unchanged,

wherein, after said zero-gain mode, said voltage-controlled oscillator operating mode is switched to a low-gain mode enabling fine tuning of the frequency of the output signal by the phase locked loop circuit to compensate for residual frequency errors and temperature variations, and

wherein the switching operation of the voltage-controlled oscillator from the zero-gain mode to the low-gain mode comprises:

using an additional element tuned by the tuning voltage that is dimensioned for fine tuning with a low voltage-controlled oscillator gain;

linking said additional element tuned by the tuning voltage to a fixed voltage during the linear-high-gain mode and the zero-gain mode;

isolating said additional element from the fixed voltage during switching from the zero-gain mode to the low-gain mode; and

linking said additional element to the tuning voltage that is supplied by the loop filter of the phase locked loop.

25. (Currently Amended) ~~Method according to claim 20,~~Method for analogue self calibrating of a phase locked loop circuit including a phase frequency detector, a charge pump, a loop filter, a voltage-controlled oscillator, including elements tuned by a tuning voltage, the method comprising:

comparing a frequency of an output signal of the voltage-controlled oscillator of the phase locked loop circuit with a reference signal frequency entering in the phase frequency detector;

switching a voltage-controlled oscillator operating mode to a linear-high-gain mode to enable a first frequency tuning operation that includes targeting a linear frequency versus voltage curve to vary the frequency of the output signal within a frequency locking range; and

after locking to a frequency with said first frequency tuning operation, switching said voltage-controlled oscillator operating mode to a zero-gain mode while keeping the frequency of the output signal unchanged,

wherein, after said zero-gain mode, said voltage-controlled oscillator operating mode is switched to a low-gain mode enabling fine tuning of the frequency of the output signal by the phase locked loop circuit to compensate for residual frequency errors and temperature variations, and

wherein a loop filter output voltage of the phase locked loop circuit is compared to an upper and a lower limit by means of additional comparators during the low-gain mode; and tuning operations are restarted and the linear-high-gain mode is selected when the loop filter output voltage reaches either of the upper limit or the lower limit.

26. (Currently Amended) Method according to claim [[19]]41, wherein phase locked loop locking time during the linear-high-gain mode is adjusted by switching off a portion of the loop filter or by increasing a current of the charge pump.

27. (Currently Amended) ~~Method according to claim 20,~~Method for analogue self calibrating of a phase locked loop circuit including a phase frequency

detector, a charge pump, a loop filter, a voltage-controlled oscillator, including elements tuned by a tuning voltage, the method comprising:

comparing a frequency of an output signal of the voltage-controlled oscillator of the phase locked loop circuit with a reference signal frequency entering in the phase frequency detector;

switching a voltage-controlled oscillator operating mode to a linear-high-gain mode to enable a first frequency tuning operation that includes targeting a linear frequency versus voltage curve to vary the frequency of the output signal within a frequency locking range; and

after locking to a frequency with said first frequency tuning operation, switching said voltage-controlled oscillator operating mode to a zero-gain mode while keeping the frequency of the output signal unchanged,

wherein, after said zero-gain mode, said voltage-controlled oscillator operating mode is switched to a low-gain mode enabling fine tuning of the frequency of the output signal by the phase locked loop circuit to compensate for residual frequency errors and temperature variations, and

wherein the phase locked loop stability during the linear-high-gain and the low-gain modes is preserved by decreasing the current of the charge pump during the linear-high-gain mode and by increasing the current of the charge pump during the low-gain mode such that a product of the current of the charge pump and gain of the voltage-controlled oscillator remains constant.

28. (Previously Presented) Integrated circuit comprising a phase locked loop circuit including:

a detector to compare phase and frequency of a reference signal to phase and frequency of an internal feedback signal and to generate output error signals,

a charge pump to generate amounts of charges proportional to said output error signals,

a loop filter to set an analogue voltage proportional to charges accumulated in capacitors and based on said amounts of charges,

a voltage-controlled oscillator with inputs that each correspond to an element tuned by a tuning voltage, and

a gain mode switcher circuit connected between an output of the loop filter and the inputs, to enable the voltage-controlled oscillator to work successively in a linear high-gain mode and a zero-gain mode, the gain mode switcher circuit including:

offset generators to generate output voltages after shifting an output voltage of the loop filter with predefined offsets,

comparators, and

a switch configuration to apply the output voltages of the offset generators to the inputs of the voltage-controlled oscillator during the linear-high-gain mode, to isolate the inputs of the voltage-controlled oscillator from the offset generators and to apply the output voltages of said offset generators to inputs of the comparators during transition to the zero-gain mode, to apply the resulting outputs voltages of said comparators to the inputs of the voltage-controlled oscillator and to freeze the state of each comparator and output frequency of the voltage-controlled oscillator making the

output frequency independent of the output voltage of the loop filter during the zero-gain mode.

29. (Previously Presented) Integrated circuit comprising a phase locked loop circuit according to claim 28, wherein the elements tuned by the tuning voltage include varactors dimensioned such that the voltage-controlled oscillator has a constant voltage to frequency gain during the linear-high-gain mode, and wherein each of the varactors is controlled by a corresponding input of the voltage-controlled oscillator.

30. (Previously Presented) Integrated circuit comprising a phase locked loop circuit according to claim 29, wherein the voltage-controlled oscillator further comprises an additional varactor for fine frequency tuning during the low-gain mode and a switch configuration that enables the application of a constant voltage to said additional varactor during the linear-high-gain mode and the zero-gain mode, and the application of the output voltage of the loop filter to said additional varactor during the low-gain mode.

31. (Previously Presented) Integrated circuit comprising a phase locked loop circuit according to claim 28, wherein the voltage-controlled oscillator includes a current controlled oscillator which includes elements tuned by the tuning voltage comprising voltage to current converters including voltage controlled current sources dimensioned such that the current controlled oscillator has a constant voltage to

frequency gain during the linear-high-gain mode, each of the voltage controlled current sources controlled by a corresponding input of the voltage-controlled oscillator.

32. (Previously Presented) Integrated circuit comprising a phase locked loop circuit according to claim 31, wherein each of the elements tuned by the tuning voltage further comprises an additional controlled current source that enables fine frequency tuning during the low-gain mode and a switch configuration that enables application of a constant voltage to said voltage controlled current sources during the linear-high-gain mode and the zero-gain mode, and the application of the output voltage of the loop filter to said additional controlled current source during the low-gain mode.

33. (Previously Presented) Integrated circuit comprising a phase locked loop circuit according to claim 28, further comprising a lock detector that activates the switch configuration such that: the linear-high-gain mode is selected during a time period for the phase lock loop circuit to lock onto a frequency,

wherein the transition to the zero-gain mode is activated after the phase lock loop circuit is locked.

34. (Previously Presented) Integrated circuit comprising a phase locked loop circuit according to claim 30, further comprising comparators that set an upper and a lower limit for the loop filter output voltage during the low-gain mode and restart the initial linear-high-gain mode when said loop filter output voltage reaches either of these two limits.

35. (Previously Presented) Integrated circuit comprising the phase locked loop circuit according to claim 28, further comprising a voltage doubler circuit that increases the voltage supply of the charge pump, the loop filter and the offset generators during the linear high-gain mode and that adjusts a tuning range of the phase locked loop circuit.

36. (Previously Presented) Integrated circuit comprising the phase locked loop circuit according to claim 35, further comprising a switch configuration enabling the application of the voltage doubler circuit to the charge pump, the loop filter and the offset generators during the linear high-gain mode.

37. (Currently Amended) The method of claim [[19]]41 wherein said voltage-controlled oscillator maintains a constant gain when operating in said linear-high-gain mode.

38. (Currently Amended) The method of claim [[19]]41 wherein said voltage-controlled oscillator maintains a constant frequency versus voltage relationship based on said linear frequency versus voltage curve to maintain a constant gain when operating in said linear-high-gain mode.

39. (Currently Amended) The method of Claim [[19]]41 further comprising generating the tuning voltage to maintain a constant gain and a constant frequency versus voltage relationship based on said linear frequency versus voltage curve.

40. (Currently Amended) ~~The method of Claim 39 further comprising:~~ Method for analogue self calibrating of a phase locked loop circuit including a phase frequency detector, a charge pump, a loop filter, a voltage-controlled oscillator, including elements tuned by a tuning voltage, the method comprising:

comparing a frequency of an output signal of the voltage-controlled oscillator of the phase locked loop circuit with a reference signal frequency entering in the phase frequency detector;

switching a voltage-controlled oscillator operating mode to a linear-high-gain mode to enable a first frequency tuning operation that includes targeting a linear frequency versus voltage curve to vary the frequency of the output signal within a frequency locking range;

after locking to a frequency with said first frequency tuning operation, switching said voltage-controlled oscillator operating mode to a zero-gain mode while keeping the frequency of the output signal unchanged;

generating a control voltage based on said comparing of said output signal and said reference signal; and

offsetting said control voltage to generate an output voltage based on said linear frequency versus voltage curve,

wherein the tuning voltage is generated based on said output voltage and a reference voltage.

41. (Currently Amended) ~~The method of claim 19 further comprising:~~ Method for analogue self calibrating of a phase locked loop circuit including a phase

frequency detector, a charge pump, a loop filter, a voltage-controlled oscillator, including elements tuned by a tuning voltage, the method comprising:

comparing a frequency of an output signal of the voltage-controlled oscillator of the phase locked loop circuit with a reference signal frequency entering in the phase frequency detector;

switching a voltage-controlled oscillator operating mode to a linear-high-gain mode to enable a first frequency tuning operation that includes targeting a linear frequency versus voltage curve to vary the frequency of the output signal within a frequency locking range;

after locking to a frequency with said first frequency tuning operation, switching said voltage-controlled oscillator operating mode to a zero-gain mode while keeping the frequency of the output signal unchanged;

generating a control voltage based on said comparing of said output signal and said reference signal; and

offsetting said control voltage to generate an output voltage,

wherein the tuning voltage is generated based on said output voltage and a reference voltage.

42. (Currently Amended) ~~The method of claim 19 further comprising:~~Method for analogue self calibrating of a phase locked loop circuit including a phase frequency detector, a charge pump, a loop filter, a voltage-controlled oscillator, including elements tuned by a tuning voltage, the method comprising:

comparing a frequency of an output signal of the voltage-controlled oscillator of the phase locked loop circuit with a reference signal frequency entering in the phase frequency detector;

switching a voltage-controlled oscillator operating mode to a linear-high-gain mode to enable a first frequency tuning operation that includes targeting a linear frequency versus voltage curve to vary the frequency of the output signal within a frequency locking range;

after locking to a frequency with said first frequency tuning operation, switching said voltage-controlled oscillator operating mode to a zero-gain mode while keeping the frequency of the output signal unchanged;

generating a control voltage based on said comparing of said output signal and said reference signal;

varying offset of said control voltage to generate a plurality of output voltages; and

generating a plurality of tuning voltages based on said plurality of output voltages and a reference voltage.

43. (Cancelled).

44. (Currently Amended) ~~The method of claim 19~~ Method for analogue self calibrating of a phase locked loop circuit including a phase frequency detector, a charge pump, a loop filter, a voltage-controlled oscillator, including elements tuned by a tuning voltage, the method comprising:

comparing a frequency of an output signal of the voltage-controlled oscillator of the phase locked loop circuit with a reference signal frequency entering in the phase frequency detector;

switching a voltage-controlled oscillator operating mode to a linear-high-gain mode to enable a first frequency tuning operation that includes targeting a linear frequency versus voltage curve to vary the frequency of the output signal within a frequency locking range; and

after locking to a frequency with said first frequency tuning operation, switching said voltage-controlled oscillator operating mode to a zero-gain mode while keeping the frequency of the output signal unchanged,

wherein said zero-gain mode comprises:

comparing an offset control voltage to a reference voltage; and

setting the tuning voltage to one of a plurality of voltage potentials based on said comparing.

45. (Currently Amended) The method of claim [[19]]41 wherein said zero-gain mode comprises maintaining a constant capacitance in said voltage-controlled oscillator.